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<u>L8</u>	L7 and ((table or map\$4) near8 (access\$4 near4 (right or permi\$6 or grant\$4)))	38	<u>L8</u>
<u>L7</u>	L6 and ((ID or identif\$8 or descri\$6) near6 (stor\$3 or input\$3 or obtain\$4 or extract\$4 or retriev\$4))	849	<u>L7</u>
<u>L6</u>	L5 and ((table or map\$4) near8 (ID or identif\$8 or descri\$6))	1129	<u>L6</u>
<u>L5</u>	L4 and ((task or process or resource or application) near8 (ID or identif\$8 or descri\$6))	2453	<u>L5</u>
<u>L4</u>	(address near6 (expan\$4 or exten\$4))	9106	<u>L4</u>
<u>L3</u>	l2 and (address near4 (expan\$4 or exten\$4))	0	<u>L3</u>
<u>L2</u>	L1 and (table or descri\$6 or identif\$6 or ID or register)	4	<u>L2</u>
<u>L1</u>	(5469556 or 5758060 or 5805879 or 6091414).pn.	4	<u>L1</u>

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DB=USPT; PLUR=YES; OP=ADJ

<u>L17</u>	L16 and ((task or process) near4 access\$4 near8 (ID or identification or identify\$4 or descri\$6))	28	<u>L17</u>
<u>L16</u>	(cpu or processor) near4 (ID or identification or identify\$4 or descri\$6) near8 (extract\$4 or retriev\$4 or obtain\$4 or remov\$4)	823	<u>L16</u>
<u>L15</u>	(cpu or processor) near4 (ID or identification or identify\$4 or descri\$6) near4 (extract\$4 or retriev\$4 or obtain\$4 or remov\$4)	639	<u>L15</u>
<u>L14</u>	L13 and l6	9	<u>L14</u>
<u>L13</u>	L12 and l11	260	<u>L13</u>
<u>L12</u>	address near4 (exten\$4 or expan\$4)	7116	<u>L12</u>
<u>L11</u>	L10 and ((previous\$2 or prior or before) near4 (address or ID or identification or identify\$4 or descri\$6))	1090	<u>L11</u>
<u>L10</u>	L9 and l8 and l7	1985	<u>L10</u>
<u>L9</u>	table near8 (defin\$6 or right or grant\$4 or permi\$6)	54904	<u>L9</u>
<u>L8</u>	(register or buffer or storage or memory) near8 (ID or identification or identify\$4 or descri\$6)	72579	<u>L8</u>
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<u>L2</u>	((711/2 711/154 711/163 711/164)!.CCLS.)	1704	<u>L2</u>
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<u>L10</u>	L9 and ((task or process or thread or resource) near4 (ID or identification or identif\$6 or descri\$6))	7	<u>L10</u>
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<u>L9</u>	((right or permi\$6 or grant\$3 or privileg\$4) near8 ((interrupt\$4 or exception or fault) near4 number))	106	<u>L9</u>
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DB=USPT; PLUR=YES; OP=ADJ

<u>L8</u>	L7 and ((table or map\$4) near8(defin\$6 or right or grant\$3 or permi\$6))	8	<u>L8</u>
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<u>L7</u>	L6 and ((task or process or thread or resource) near4 (ID or identification or identif\$6 or descri\$6))	19	<u>L7</u>
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<u>L6</u>	((right or permi\$6 or grant\$3 or privileg\$4) near8 ((interrupt\$4 or exception or fault) near4 number))	183	<u>L6</u>
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DB=PGPB,JPAB,EPAB,DWPI,TDBD; PLUR=YES; OP=ADJ

<u>L5</u>	L4 and ((right or permi\$6 or grant\$3 or privileg\$4) near8 ((interrupt\$4 or exception or fault) near4 number))	1	<u>L5</u>
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<u>L4</u>	(address adj2 space) near4 (exten\$4 or expan\$4)	403	<u>L4</u>
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DB=USPT; PLUR=YES; OP=ADJ

<u>L3</u>	L1 and ((right or permi\$6 or grant\$3 or privileg\$4) near8 ((interrupt\$4 or exception or fault) near4 number))	3	<u>L3</u>
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<u>L2</u>	L1 and (((access\$4 or read\$4 or writ\$4 or stor\$3 or load\$3) near3 (right or permi\$6 or grant\$3 or privileg\$4)) near8 ((interrupt\$4 or exception) near4 number))	0	<u>L2</u>
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<u>L1</u>	(address adj2 space) near4 (exten\$4 or expan\$4)	583	<u>L1</u>
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| | Alberto Belussi , Christos Faloutsos
ACM Transactions on Information Systems (TOIS) April 1998
Volume 16 Issue 2
The problem of selectivity estimation for queries of nontraditional databases is still an open issue. In this article, we examine the problem of selectivity estimation for some types of spatial queries in databases containing real data. We have shown earlier [Faloutsos and Kamel 1994] that real point sets typically have a nonuniform distribution, violating consistently the uniformity and independence assumptions. Moreover, we demonstrated that the theory of ... | |
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| | D. A. Wood , S. J. Eggers , G. Gibson , M. D. Hill , J. M. Pendleton
ACM SIGARCH Computer Architecture News , Proceedings of the 13th annual international symposium on Computer architecture June 1986
Volume 14 Issue 2
In the design of SPUR, a high-performance multiprocessor | |

workstation, the use of large caches and hardware-supported cache consistency suggests a new approach to virtual address translation. By performing translation in each processor's virtually-tagged cache, the need for separate translation lookaside buffers (TLBs) is eliminated. Eliminating the TLB substantially reduces the hardware cost and complexity of the translation mechanism and eliminates the translation consistency problem. Trac ...

4 An analysis of errors and their causes in system programs 98%


 Albert Endres

ACM SIGPLAN Notices , Proceedings of the international conference on Reliable software April 1975

Volume 10 Issue 6

Program errors detected during internal testing of the operating system DOS/VS form the basis for an investigation of error distributions in system programs. Using a classification of the errors according to various attributes, conclusions can be drawn concerning the possible causes of these errors. The information thus obtained is applied in a discussion of the most effective methods for the detection and prevention of errors.

5 801 storage: architecture and programming 98%

 Albert Chang , Mark F. Mergen

ACM Transactions on Computer Systems (TOCS) February 1988

Volume 6 Issue 1

Based on novel architecture, the 801 minicomputer project has developed a low-level storage manager that can significantly simplify storage programming in subsystems and applications. The storage manager embodies three ideas: (1) large virtual storage, to contain all temporary data and permanent files for the active programs; (2) the innovation of database storage, which has implicit properties of access serializability and atomic update, similar to those o ...

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